CLAIMS

What is claimed is:

1. A method comprising:

forming a layer of porous silicon on a top surface of a silicon substrate;

depositing a layer of silicon on the layer of porous silicon;

forming a device layer of an integrated circuit device within the layer of silicon;

bonding a temporary support layer to the device layer;

splitting the porous silicon layer;

removing any portion of the porous silicon layer from the silicon layer; and

removing the temporary support layer from the device layer.

2. The method of claim 1 further comprising:

packaging the device layer using standard integrated circuit packaging; and

bonding the thin device layer to an integrated heat spreader.

3. The method of claim 1 wherein the silicon layer is approximately 10 - 50 microns thick and the device layer is approximately 0.1 – 1 micron thick.

4. The method of claim 1 wherein the layer of porous silicon is formed using an anodization process.

5. The method of claim 1 wherein the support layer is bonded to the device layer using adhesive.

6. The method of claim 1 wherein the support layer is plastic.

7. The method of claim 1 wherein polishing is used to remove any portion of the porous silicon layer from the silicon layer.

8. An apparatus comprising:

a silicon substrate;

a layer of porous silicon formed upon the substrate;

a layer of polysilicon deposited upon the layer of porous silicon;

an insulator layer bonded to the layer of polysilicon; and

a silicon layer disposed upon the insulator layer.

9. The apparatus of claim 8 wherein the layer of porous silicon is a variable-density porous silicon layer having a relatively higher density near the silicon substrate and a relatively lower density near the polysilicon layer.

10. The apparatus of claim 8 wherein the silicon layer is approximately 10 - 50 microns thick and the device layer is approximately 0.1 – 1 micron thick.

11. The apparatus of claim 8 wherein the layer of porous silicon is formed using an anodization process.

12. The apparatus of claim 11 wherein the anodization process is effected by dissolving a bulk silicon wafer in an electromechanical cell containing a hydrogen fluoride solution.

13. The apparatus of claim 8 wherein the insulator layer is an oxide layer.

14. A method of forming a silicon-on-insulator-on-porous-silicon (Si/I/pSi) wafer comprising:

forming a porous silicon layer on a silicon substrate;

depositing a polysilicon layer on the porous silicon layer;

implanting a H_2 layer within a donor wafer such that the donor wafer has a surface silicon layer;

depositing an insulator layer on the surface silicon layer of the donor wafer;

bonding the insulator layer to the polysilicon layer to create a bonded pair; and

splitting the bonded pair through the H2 implanted layer in donor wafer leaving a portion of the silicon layer disposed upon the insulator layer to form a silicon layer of the Si/I/pSi wafer.

15. The method of claim 14 the porous silicon layer is a variable-density porous silicon layer having a relatively higher density near the silicon substrate and a relatively lower density near the polysilicon layer.

16. The method of claim 14 wherein the surface silicon layer is approximately 10 - 50 microns thick and the device layer is approximately 0.1 – 1 micron thick.

17. The method of claim 14 wherein the layer of porous silicon is formed using an anodization process.

18. The method of claim 17 wherein the anodization process is effected by dissolving a bulk silicon wafer in an electromechanical cell containing a hydrogen fluoride solution.

19. The method of claim 14 wherein the insulator layer is an oxide layer.

20. A method comprising:

forming a device layer of an integrated circuit device within a surface silicon layer of a silicon-on-insulator-on-porous-silicon (Si/I/pSi) wafer;

bonding a support layer to the device layer;

splitting the porous silicon layer;

removing any portion of the porous silicon layer from the silicon layer; and

removing the support layer from the device layer.

21. The method of claim 20 wherein the Si/I/pSi wafer is produced by forming a porous silicon layer on a silicon substrate, depositing a polysilicon layer on the porous silicon layer, implanting a H_2 layer within a donor wafer such that the donor wafer has a surface silicon layer, depositing an insulator layer on the surface silicon layer of the donor wafer, bonding the

insulator layer to the polysilicon layer to create a bonded pair, and splitting the bonded device through the H2 implanted layer in donor wafer leaving a portion of the silicon layer disposed upon the insulator layer to form a silicon layer of the Si/I/pSi wafer.

22. The method of claim 20 further comprising:

packaging the device layer using standard integrated circuit packaging; and

bonding the device layer to an integrated heat spreader.

23. The method of claim 21 wherein the porous silicon layer is a variable-density porous silicon layer having a relatively higher density near the silicon substrate and a relatively lower density near the surface silicon layer.

24. The method of claim 20 wherein the surface silicon layer is approximately 10 - 50 microns thick and the device layer is approximately 0.1 – 1 micron thick.

25. The method of claim 21 wherein the layer of porous silicon is formed using an anodization process effected by dissolving a bulk silicon wafer in an electromechanical cell containing a hydrogen fluoride solution.

26. The method of claim 20 wherein the support layer is a plastic layer bonded to the device layer using adhesive.

27. The method of claim 21 wherein polishing is used to remove any portion of the porous silicon layer from the silicon layer of the Si/I/pSi wafer.